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A High Speed CMOS Current Comparator at Low Input Current

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Abstract
Analysis of high speed CMOS current comparator is presented with low input impedance using a simple biasing method. The simulation results from PSPICE demonstrate the propagation delay at low input currents at supply voltages of 1.8v, 2v, 2. 2v and stability analysis using 0.25um CMOS technology. So it is suitable to high speed applications.
Keywords—Current comparators, propagation delay, positive feedback, signal processing.

I.   INTRODUCTION

Current comparators are important building blocks within many analogue circuits designs. In particular, they are used for front-end signal processing applications and increasingly within neuromorphic electronic systems [1,2]. A/D converters may be designed using current-mode technologies.   Since many digital and analog circuits have been tried to switch from voltage mode to current, mode operations. Current comparators may be the key elements. It consumes less power dissipation, achieves more dynamic range and high operation speed. Thus the current mode circuit design methodology receives increasingly wide attention in recent years [3,4].

In order to detect low current with high speed, many current comparators have been proposed. The simplest current comparator with positive feedback and low input impedance is shown in fig.1 [5] i.e. Traff current comparator. When the input current (Iin) flows into the circuit through V1, Vout is high. When input current (Iin) flows out of the circuit, Vout is low. CMOS inverters at the output stage to give rail-to-rail voltage swing. If the input current is small enough, there exists a deadband problem where the input impedance is quite high during input transition thus limiting the speed of operation.

Fig.1

For reducing the deadband region of current comparator change its biasing scheme from class B to class AB. Another approach using resistor feedback to detect small currents shown in fig.2 [6].A simple current-source inverting amplifier seems attractive for many applications, but its large output resistance prevents its use at high speed, especially for capacitive loads. High speed current comparator requires low input impedance for increased current sourcing and sinking capability. Input and output resistance can be reduced by resistive feedback in first inverting amplifier in the input stage of current comparator. More inverters are required at the output stage to produce rail-to-rail output swing. This comparator is good for high speed at low input current but the power consumption is much higher due to constant current.

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Fig.2

II.   13TCURRENT COMPARATOR

Since the response of original current comparators degrades drastically at low input current. One of the most significant problem of deadband has been minimized. Fig.3 shows the 13T current comparator which has one diode-connected

enhance the speed. M8-M11 are the pairs of CMOS inverters to amplify the output signal. The two transistors Mp and Mn are used to adjust the inverter threshold voltage of M8 and M9 using different voltages values of Vn and Vp.

For typical case Gate of Mp i.e. Vp is connected to ground and Mn i.e. Vn is connected to Vdd.
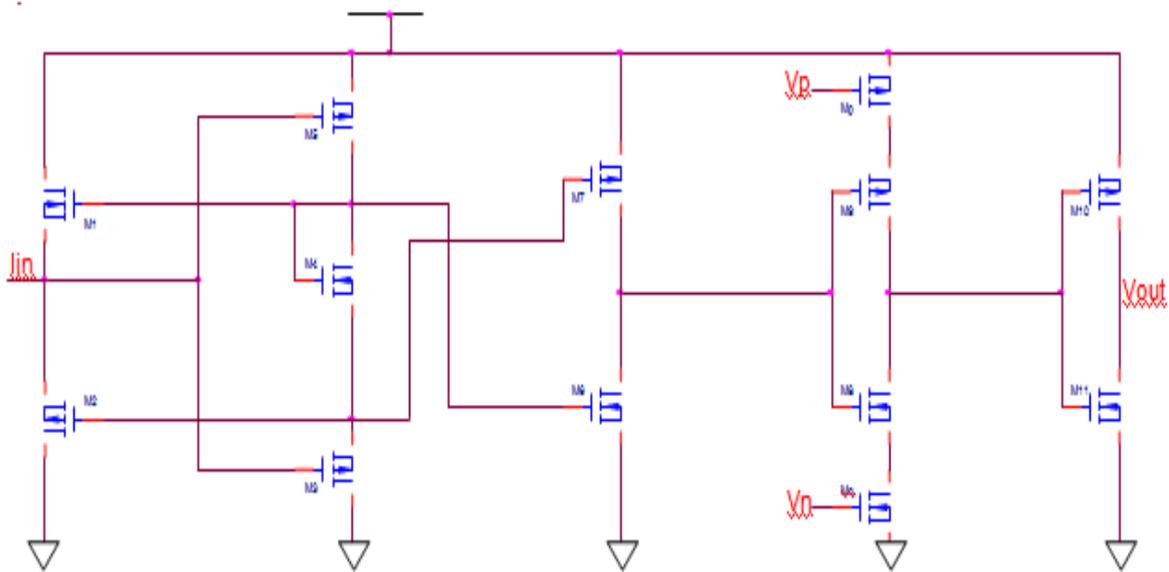
Fig.3

transistor NMOS transistor instead of using two to provide voltage drop between the gates of M1 and M2. M3 and M5 forms the reference current generating stage. Input current (Iin) is connected to the first stage of the circuit. The drain and source of M4 is connected to the gates of M6 and M7. M4 is used to give higher current for charging and discharging the gates of M8 and M9 and thus

III. PERFORMANCE ANALYSIS

The 13T current comparator is simulated for various input currents and compared with circuits of fig.[1] and fig.[2] at Vdd=1.8v,2v,2.2v using 0.25um. Fig.4,5,6 shows the transient analysis of three different current comparators. In this propagation delay of current comparators is presented. The propagation delay is defined as the difference of time

between the output and input when they reach the 50% of the total variation. The speed of 13T current comparator is much faster than other two comparators at 190uA and low power consumption is achieved at 1.8v. The resistor feedback is also good for high speed at low input current but the delay time is still longer than the 13T current comparator.

Transient analysis of Traff current comparator
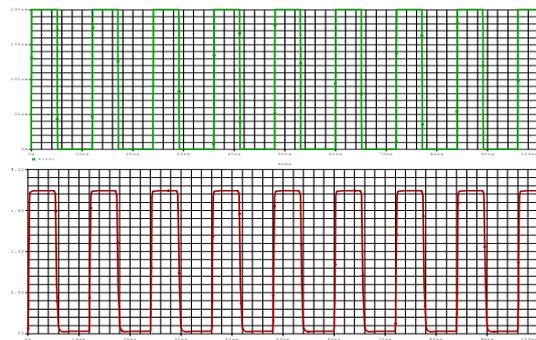
Fig.4

Transient analysis of resistor feedback current comparator
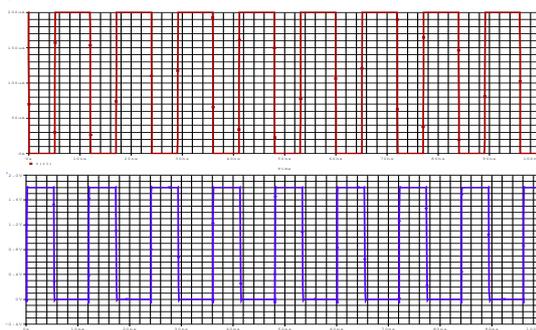
Fig.5

Transient analysis of 13T current comparator
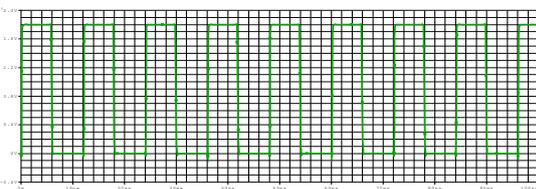
Fig.6

IV.COMPARISON TABLES

TRANSIENT ANALYSIS FOR PROPAGATION DELAY

TABLE 1:
Comparison of current comparators at Vdd=1.8v

VDD=1.8V	TRAFF CURRENT COMPARATOR	RESISTIVE FEEDBACK COMPARATOR	13T CURRENT COMPARATOR
Input current (uA)	propagation delay(ps)	propagation delay(ps)	propagation delay(ps)
190	421.466	326.5655	310.1485
195	411.7385	347.636	330.4525
200	406.1915	354.861	340.8425
205	396.9805	356.813	354.816
210	395.381	359.0665	355.914
215	386.907	384.572	385.5225
220	382.747	405.591	401.9985
225	376.164	408.2525	410.286

Graph(a) of Table1

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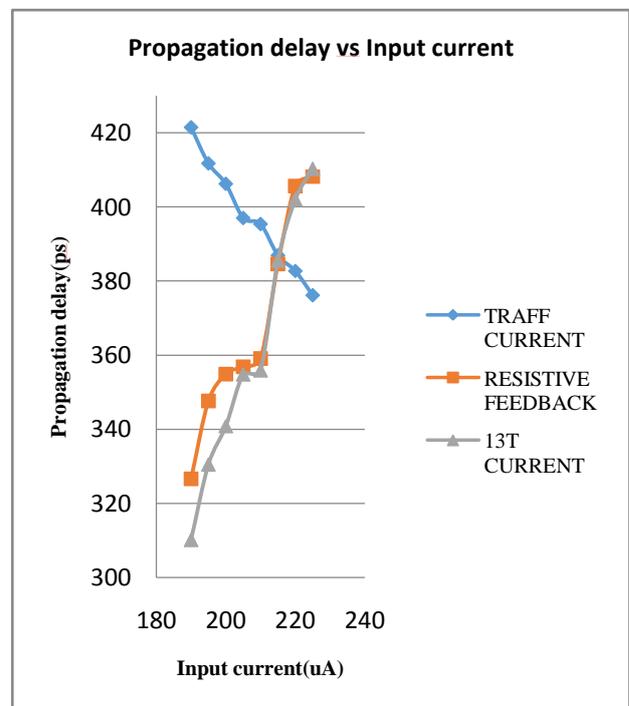
TABLE2: Comparison of current comparators at Vdd=2v

VDD =2V	TRAFF CURRENT COMPARATOR	RESISTIVE FEEDBACK COMPARATOR	13T CURRENT COMPARATOR
Input current (uA)	Propagation delay(ps)	Propagation delay(ps)	propagation delay(ps)
190	458.669	257.236	250.1485
195	455.659	298.955	284.4525
200	453.05	318.6625	315.8425
205	450.877	322.6635	315.816
210	448.6555	325.5635	320.914
215	434.4925	326.429	322.5225
220	398.7235	328.499	329.9985
225	396.5835	329.2535	331.286

TABLE 3: Comparison of current comparators at Vdd=2.2v

VDD= 2.2V	TRAFF CURRENT COMPARATOR	RESISTIVE FEEDBACK COMPARATOR	13T CURRENT COMPARATOR
Input current (uA)	propagation delay(ps)	propagation delay(ps)	propagation delay(ps)
190	334.436	327.1645	322.1485
195	331.4125	331.27	324.4525
200	324.0825	345.232	335.8425
205	313.954	356.4445	336.816
210	306.5965	357.155	342.914
215	299.647	358.0365	348.5225
220	292.1155	359.98	355.9985
225	283.0775	359.28	360.286

Graph(b) of Table 2
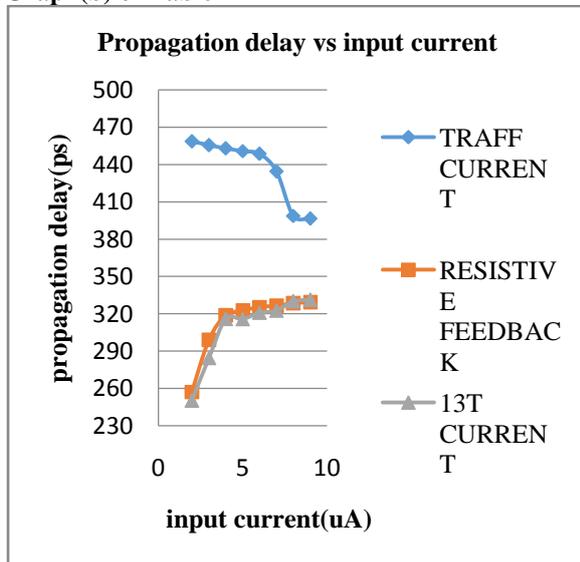
Graph(c) of Table 3
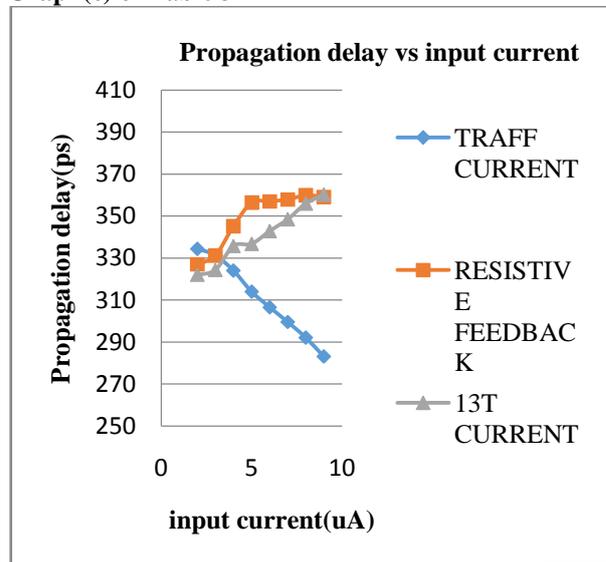
V.AC ANALYSIS FOR STABILITY
Phase margin and Gain margin of Traff current comparator
Table 1a

Traff current comparator	Phase margin	Gain margin(db)
With stability	50.45590	12.73633
Without stability	42.68272	6.30394

Phase margin and gain margin of resistor feedback current comparator
Table 1b With stability

Iin-Iref (mA)	Phase margin	Gain margin(db)
2mA(50-48)	49.99984	10.34619
4mA(50-46)	52.54245	11.33189
6mA(50-44)	53.95440	11.32349
10mA(50-40)	55.48013	11.31445

Without stability

Iin-Iref (mA)	Phase margin	Gain margin(db)
2mA(50-48)	49.99984	10.34619
4mA(50-46)	52.54245	11.33189
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10mA(50-40)	55.48013	11.31445

Phase margin and gain margin of 13T current comparator

(Without stability)
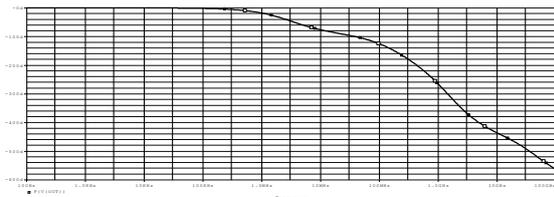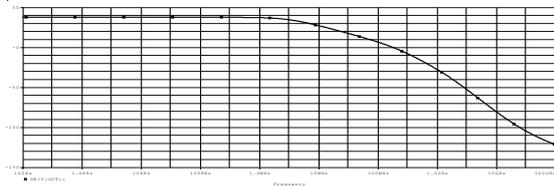
(With stability)
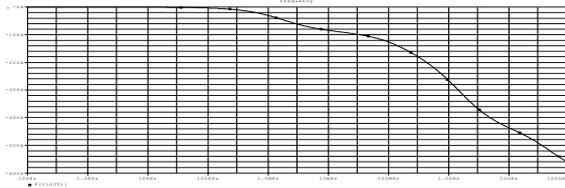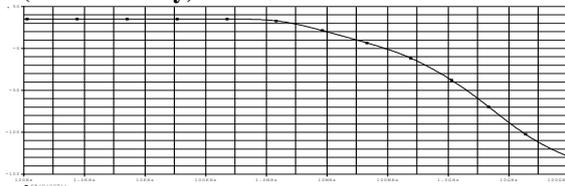
Table 1c

13T current comparator	Phase margin	Gain margin(db)
Without stability	30.14507	7.72318
With stability	48.55657	12.76250

- **POWER DISSIPATION**
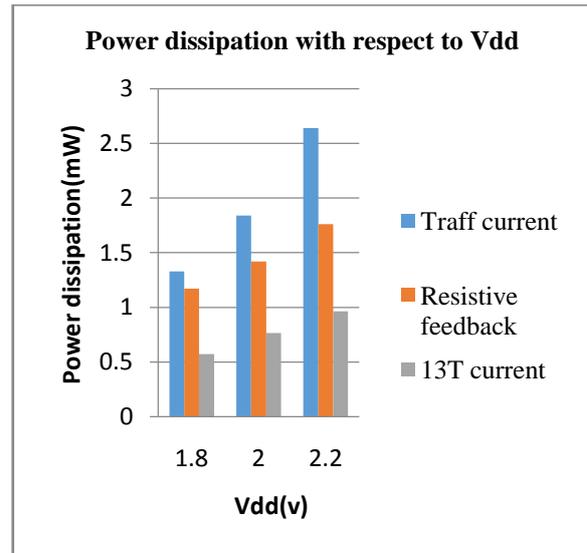
Graph (d)

Table 1,2,3 shows the propagation delay and its graph a,b,c. Table 1a, 1b, 1c shows the stability analysis of three different current comparators. Graph (d) represents the power dissipation with respect to Vdd.

VI.   CONCLUSION
In this paper a high speed CMOS current comparator is presented using simple biasing method. In addition to less number of transistors the performance is better than both the comparators. From simulated results we concluded that 13T current comparator at 2v is much stable, delay time reduces with optimum power dissipation is achieved.

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